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Nucleation and growth of gallium arsenide on silicon (1 1 1)

V. ALBERTS
Physics Department, Rand Afrikaans University, PO Box 524, Aucklandpark, Johannesburg 2006, South Africa

J. H. NEETHLING, J. S. VERMAAK
University of Port Elizabeth, Physics Department, PO Box 1600, Port Elizabeth 6000, Republic of South Africa

The nucleation and growth of undoped gallium arsenide (GaAs) epitaxial layers, grown by metalorganic vapour phase epitaxy (MOVPE) on Si (1 1 1) substrates were investigated by transmission electron microscopy (TEM). The initial stages of epitaxial growth are considered at high and low growth temperatures. The influence of growth time and thermal annealing on the initial stages of growth are also studied and reported.

1. Introduction

The hetero-epitaxial growth of GaAs on Si substrates offers tantalizing advantages for high-speed integrated circuits, and is currently the subject of intense activity [1]. However, GaAs epilayers with high crystalline quality are difficult to obtain. This is because the hetero-epitaxial growth of GaAs on Si has problems such as a large lattice mismatch (4%), the difference (55%) of thermal expansion coefficients and antiphase domains. Three-dimensional growth, which always occurs at the initial growth stage, could also degrade the crystalline quality [2]. Dogged research has triumphed over these difficulties in recent years, and has managed to produce very good quality GaAs epilayers on silicon. Important techniques which have led to the growing of high quality GaAs include the use of tilted silicon substrates [3], post and *in situ* annealing [4] and the use of strained layer superlattices [5]. However, the most widely used method to grow GaAs/Si epitaxial layers of low-defect density is the MOVPE two-step growth technique [6]. In this procedure, a thin (10–20 nm) GaAs buffer layer is first grown at a slow growth rate before conventional GaAs homo-epitaxial growth temperature and growth rate conditions are imposed. The role of the low temperature GaAs layer is to ensure complete coverage of the Si substrate at the initial stage of growth. It has already been reported by several workers [6, 7] that the GaAs nucleation layer grows three-dimensionally on Si. Many structural defects (twins, stacking faults and dislocations) are produced during the growth and coalescence of these islands.

Although it is well-known that the crystallinity of the layer subsequently grown on the buffer layer is strongly affected by the quality and morphology of the latter, there is at present little information available on the initial stages because of the difficulties involved in *in situ* observations.

In a previous study [8] we presented direct observation of the nucleation and growth of thin (10–40 nm) GaAs nucleation layers on (0 0 1) Si. Planar view TEM studies indicated that GaAs nucleated as three-dimensional islands on (0 0 1) Si and eventually coalesced into a continuous epitaxial film as growth proceeded. High twin densities were observed in the thin (0 0 1) GaAs nucleation layers. The twin structures were revealed by the presence of reflections, other than the allowed and expected matrix reflections, and double diffraction spots in the selected area diffraction (SAD) patterns. A detailed analysis of the (0 0 1) SAD pattern [9] revealed that these twin spots occur as a result of primary and tertiary twinning on the {1 1 1} planes of GaAs.

In this paper, transmission electron microscopy (TEM) results of a study of the nucleation and growth of GaAs on (1 1 1) Si, are presented. The initial stages of epitaxial growth at high (650 °C) and low (450 °C) temperatures are considered. The influence of growth time and thermal annealing on the crystallinity and defect density of the nucleation layers is also considered and reported in this paper.

2. Experimental procedure

The GaAs layers were grown on *n*-type 10 Ω cm (1 1 1) Si substrates in an MOVPE system at atmospheric pressure. Substrates were degreased and dipped in a diluted hydrofluoric acid solution, prior to introduction to the MOVPE growth reactor. The chemically cleaned Si (1 1 1) substrates were heated at 850 °C for 20 min in an AsH_3 and H_2 ambient to remove traces of oxide residue. Subsequently, the clean Si surfaces were exposed to AsH_3 flux at 450 °C for 2 min. This deposition of arsenic on Si results in a well-ordered, highly passivated and stable surface [10], which is essential for the growth of single-domain GaAs. The

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source chemicals used throughout this work include trimethylgallium (TMG) and 10% AsH_3 in H_2. The carrier gas was palladium-diffused H_2, and the total gas flow rate was kept constant at 2150 $cm^3 min^{-1}$. With a TMG flow rate of 7.5 $cm^3 min^{-1}$ and V/III ratio of 70, the GaAs buffer layers were subsequently grown at 650 and 450 °C. The average growth rate under these growth conditions was $\sim 0.4 nm s^{-1}$. These buffer layers were then annealed at 720 °C for 10 min in a H_2 and AsH_3 atmosphere. The defect structure and crystalline quality of the GaAs nucleation layers were studied by means of plan and cross-sectional view TEM. The samples for TEM observation were prepared by mechanical thinning followed by ion milling. The morphology of the grown samples was studied by Nomarski interference microscopy.

3. Results and discussion

In the present study the influence of growth temperature, growth time and thermal annealing on the initial stages of MOVPE growth of GaAs on (1 1 1) Si, is studied by TEM. Fig. 1a shows a Nomarski optical micrograph of a GaAs nucleation layer, grown on (1 1 1) Si at 650 °C for 120 s. This micrograph clearly reveals the rough surface structure of this high-temperature grown GaAs layer on Si (1 1 1). The rough surface structure of this layer can be explained by considering the effect of growth temperature on the size and density of the GaAs islands. Several workers [11] reported that the island size and separation increased, while the island density decreased as the growth temperature was increased. It is, therefore, expected that GaAs islands grown at high temperatures (650 °C) on Si (1 1 1) will be very large in size; which also corresponds to very low island densities. This behaviour is consistent with a model where surface transport becomes dominant over nucleation as the growth temperature increases. The degradation of surface morphology with increasing growth temperature can, therefore, be ascribed to the nucleation of large GaAs islands on the Si substrates during growth. It will be shown in this paper that these rough surface morphologies of the GaAs epilayers, grown at a high temperature on Si (1 1 1), correspond to high defect densities in these layers. Fig. 2 shows cross-sectional and planar views with a corresponding $(\bar{1}\,\bar{1}\,\bar{1})$ diffraction pattern of the GaAs nucleation layer, grown on Si (1 1 1) at 650 °C. The cross-sectional view in Fig. 2a clearly shows the poor thickness uniformity of this layer, which is in agreement with the rough surface morphology revealed by Nomarski studies. The GaAs layer thickness was measured at different points across the layer surface, yielding a minimum and maximum value of 150 and 800 nm, respectively. Several inclined growth defects are also clearly visible in the cross-sectional TEM image in Fig. 2a. The lattice defects present in this layer are mainly 60 ° dislocations (D) and columnar-type microtwinned crystals (T). Fig. 2b is a bright-field planar view TEM micrograph of the GaAs epilayer grown directly on Si (1 1 1) at 650 °C. The large grains responsible for the rough surface morphology of this layer are clearly visible in this micrograph. The fringes visible in this figure are produced by the twin boundaries. Fig. 2c shows the SAD pattern obtained from this (1 1 1) layer. This complex diffraction pattern indicates the GaAs main diffraction spots and twin spots. In this diffraction pattern, shown in Fig. 2c, the six (2 2 0) GaAs main diffraction spots are indexed. The streaking around the (2 2 0) spots are produced by higher order (2 2 2) reflections from secondary twinned crystals; because the (2 2 2) secondary twin reflections do not lie on the Ewald sphere, only the streaks are visible. Double diffraction at twin boundaries is responsible for the presence of six streaks around each (2 2 0) matrix reflection. For certain orientations, a (2 2 2) secondary twin reflection may be tilted towards a reflecting condition. This is also indicated in Fig. 2c, where a (2 2 2) reflection is indicated by T. Also evident in this diffraction pattern are the twelve (1 1 1) secondary twin spots, consisting of six pairs of adjacent (1 1 1) spots, lying at an angular distance of 6 ° apart from each other. One such pair is indicated by A in Fig. 2c. Also clearly visible in Fig. 2c are the twelve (1 1 1) secondary twin spots, consisting of six pairs of adjacent (1 1 1) spots (two of which are indicated by B). These twin spots (B) lie at an angular distance of 10 ° apart from each other. A detailed analysis of this (1 1 1) diffraction pattern is presented elsewhere [9]. Another very important feature of this diffraction pattern is the presence of well-defined GaAs matrix spots, which indicate that this high-temperature grown GaAs layer on Si (1 1 1) at 650 °C is single crystalline. It can, therefore, be concluded from this diffraction pattern given in Fig. 2c that, although the layers grown directly on Si (1 1 1) at a high temperature are single crystalline, these layers are also heavily twinned. Fig. 2d shows a dark-field planar view TEM micrograph of a slightly different area of the same sample shown in Fig. 2b. This dark-field image, obtained by using a secondary twin spot indicated by A in Fig. 2c, confirms the initial inference that some of these large grains, observed in (b), are

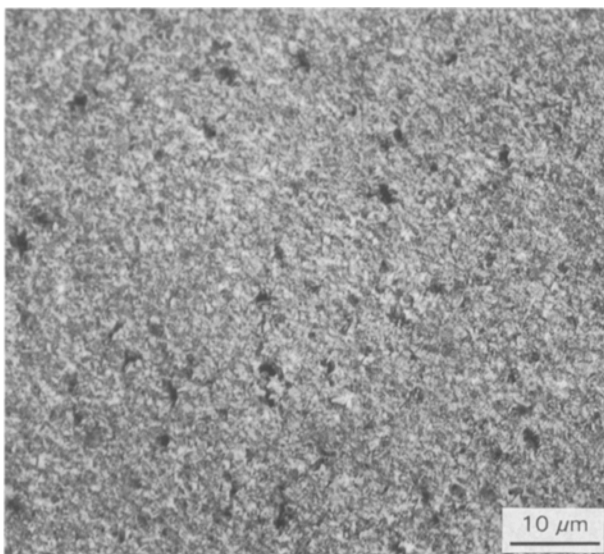
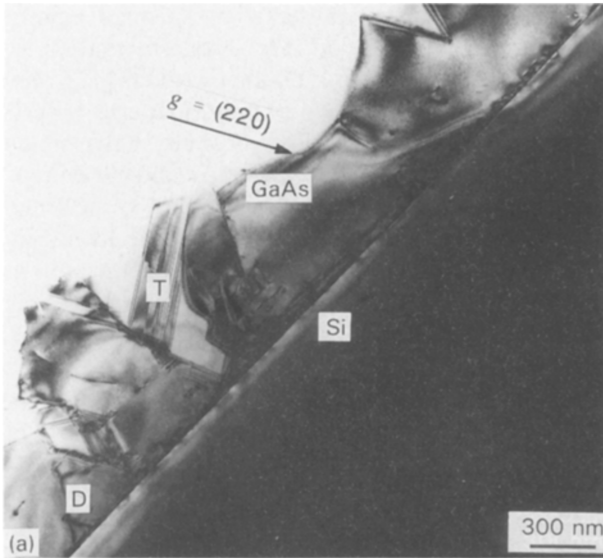
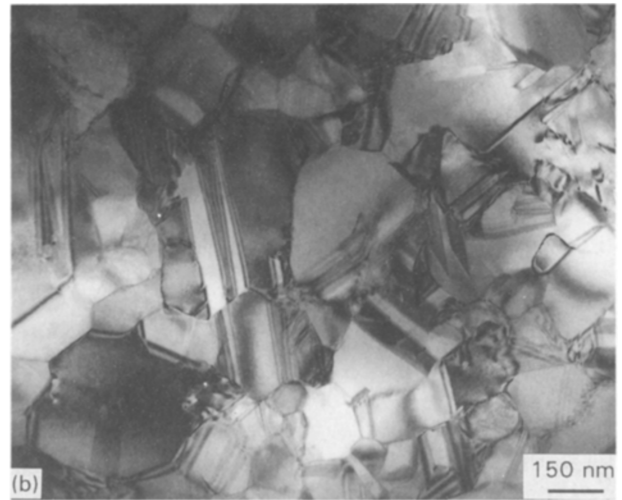


Figure 1 Nomarski microphotograph of the surface morphology of a GaAs layer, grown on Si (1 1 1) at 650 °C for 120 s.





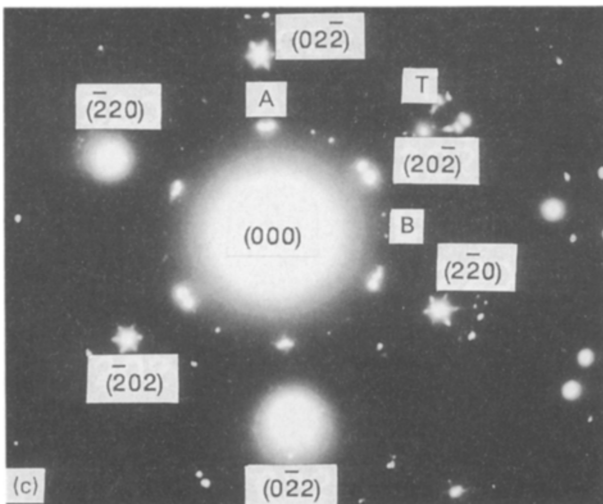
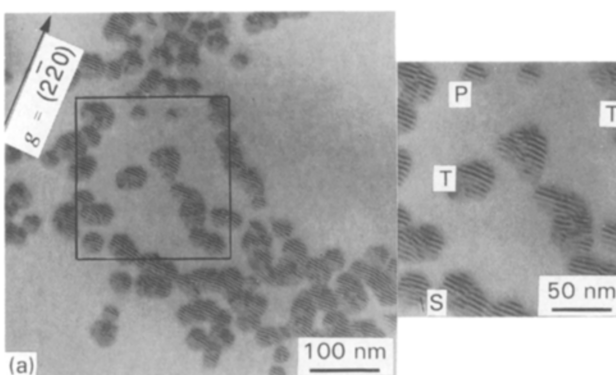


Figure 2 (a) Bright-field cross-sectional TEM micrograph of a MOVPE GaAs/Si (1 1 1) interface of GaAs grown on (1 1 1) Si at 650 °C for 120 s. The electron beam is close to the (1 $\bar{1}$ 1). (b) Bright-field planar view TEM micrograph of a GaAs layer grown on Si (1 1 1) at 650 °C for 120 s, and (c) corresponding SAD pattern. The electron beam is close to the ($\bar{1}$ $\bar{1}$ $\bar{1}$). (d) Dark-field planar view TEM micrograph, obtained from a secondary twin spot, indicated by A in (c).

microtwinned crystallites. The large twinned islands present in these high-temperature grown layers (see Fig. 2b) lead to rough surface morphologies, as can be seen from Fig. 2a.

In the second part of this study TEM results are presented of low-temperature MOVPE grown GaAs nucleation layers on (1 1 1) Si. In order to study the initial stages of growth, GaAs buffer layers were grown on Si (1 1 1) at 450 °C, using nucleation growth times of 45, 60, 75, 90 and 120 s. These buffer layers were then annealed at 720 °C for 10 min. Fig. 3a shows a bright-field planar view TEM micrograph of an as-grown GaAs buffer layer, grown for 45 s on (1 1 1) Si, at 450 °C. This micrograph clearly indicates



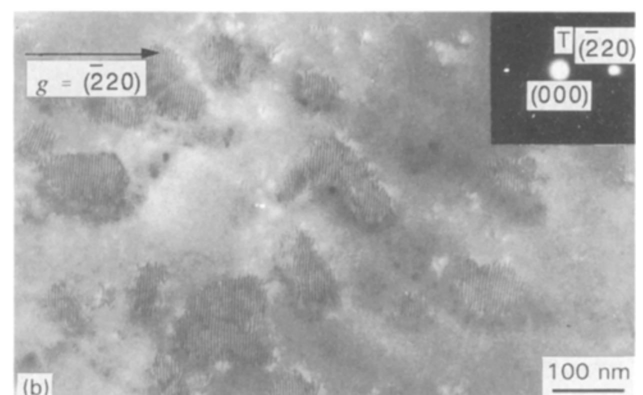


Figure 3 Bright-field planar view TEM micrographs and corresponding SAD patterns of undoped MOVPE (a) as-grown (450 °C for 45 s) and (b) annealed (720 °C for 10 min) GaAs buffer layers on (1 1 1) Si for a growth time of 45 s. The electron beam is close to the ($\bar{1}$ $\bar{1}$ $\bar{1}$) direction.

that the initial growth stage of the surface film consists of a dispersion of small three-dimensional islands, covering the Si (1 1 1) surface. The most obvious feature of this micrograph is the region of moiré fringe contrast, which identifies regions with epitaxial oriented GaAs. These parallel moiré fringes, perpendicular to the $g = (\bar{2}\,2\,0)$ operating reflection, are produced by the two overlapping GaAs and Si crystals with different lattice spacings and in parallel orientation. The measured spacing of the moiré fringes, shown in Fig. 3a [obtained for a (2 2 0) reflection], is equal to 4.7 ± 0.2 nm. This value is in good agreement with the theoretical value of 5 nm and demonstrates the recovery of the GaAs lattice to the bulk value, although the GaAs layer is grown on a highly lattice mismatched Si substrate. An enlargement of a region framed by a square black line in Fig. 3a is inserted next to this figure. Double-positioned islands (some of which are indicated by T) are clearly evident in this enlargement. The presence of these double-positioning boundaries in this layer is an indication that this epitaxial overgrowth is the result, not only of epitaxial nucleation, but of reorientation processes during growth. The different orientations in these double-positioned islands are represented by the small regions without moiré fringe contrast. This observation is consistent with the findings of other workers [12] who suggested that the direction of moiré patterns is very sensitive to the alignment of two crystals, so that small local misalignments can be detected and measured. These moiré patterns are also very useful in the sense that they allow lattice imperfections to be identified [13]. It is important to note, that if a stacking fault or thin twin is present in these islands, one observes a displacement of moiré fringes across the projected width of the fault. Such a stacking fault is indicated by S in the enlarged area in Fig. 3a. Discrete islands (have not coalesced with neighbouring islands) with a typical diameter of 20 nm are also visible in Fig. 3a. The moiré fringes covering these initial islands (indicated by P) are undisturbed, and, therefore, indicate that no lattice imperfections are present in the initial nuclei of the deposit. Fig. 3b is a planar view TEM micrograph of a GaAs buffer layer grown for 45 s on Si (1 1 1) and then annealed at 720 °C for 10 min. This micrograph clearly differs from the previous one, showing the presence of a low density of large GaAs islands. It, therefore, appears that the annealing process led to an

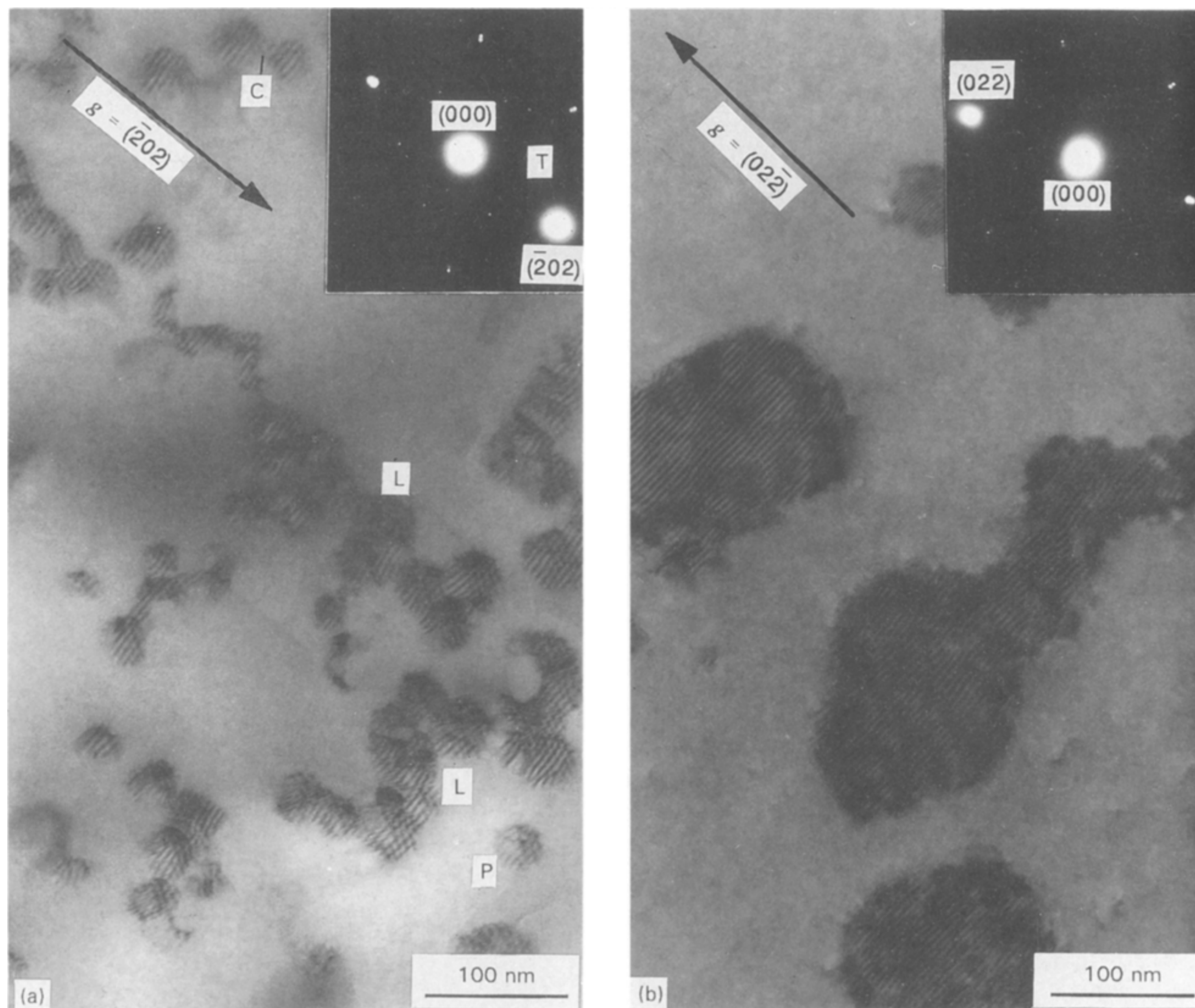


Figure 4 Bright-field planar view TEM micrographs and corresponding SAD patterns of undoped MOVPE (a) as-grown (450 °C) and (b) annealed (720 °C) GaAs buffer layers on (1 1 1) Si for a growth time of 60 s. The electron beam is close to the $(\bar{1}\,\bar{1}\,\bar{1})$ direction.

increase in the mean radius and dispersion of the islands, while decreasing the number of islands per unit area. This phenomenon, generally known as Oswald ripening [14], has also been observed during the annealing of GaAs islands on (0 0 1) Si [8] and occurs because at least some of the nuclei of all sizes achieve a degree of mobility on the Si surface when the temperature is raised. This subsequently leads to the growth of large nuclei at the expense of the smaller ones. It can also be seen from Fig. 3b that most of the compound islands still have rounded profiles after annealing. It is also important to notice that the moiré fringes, covering the GaAs islands in Fig. 3a and b, are distorted as a result of lattice defects (twins and dislocations) present in the islands. From a comparison of Fig. 3a and b it can, however, be seen that the moiré fringes are more regular after annealing; indicating that the overall orientation of the layer improves with annealing. The inset SAD pattern in Fig. 3b, showing the Si and GaAs main diffraction spots, verifies that perfect epitaxy exists between the substrate and deposit with the orientation relationship.

$$\{1\,1\,1\}_{GaAs} \| \{1\,1\,1\}_{Si}$$

and

$$\langle 1\,\bar{1}\,0\rangle_{GaAs} \| \langle 1\,\bar{1}\,0\rangle_{Si}$$

Also present in the SAD pattern are faint (1 1 1) twin spots (T). A detailed analysis of this SAD pattern is published elsewhere [9].

Fig. 4a is a planar TEM view of an as-grown buffer layer grown for 60 s at 450 °C on Si (1 1 1). The liquid-like coalescence of nuclei and islands which take place as nuclei or islands touch each other, leads to the formation of large elongated island structures (indicated by L in Fig. 4a). It is clearly evident from this micrograph that the initial nuclei (P) before coalescence have rounded profiles with typical diameters of 40 nm. The coalescence of a pair of rounded islands, which leads to the formation of a neck between these islands, is indicated by C in Fig. 4a. This neck formation is the first step in the coalescence of islands. It can again be seen from Fig. 4b that thermal annealing at 720 °C for 10 min increased the mean size and dispersion of the islands, while decreasing the number of islands per unit area. The annealed islands, grown for 60 s, are larger than those grown for 45 s (see Fig. 3b), indicating that an increase in growth time led to an increase in island size. The inset SAD patterns which were taken from the as-grown and annealed GaAs buffer layers, grown for 60 s, again show the Si and GaAs main diffraction spots and (1 1 1) twin spots. These twin spots, however, become faint after annealing, suggesting that these twin structures in the thin epitaxial GaAs buffer layers are removed to a certain extent by thermal annealing.

Fig. 5a and b shows the area distribution of the as-grown (450 °C) and annealed (720 °C for 10 min) GaAs islands, respectively; grown on (1 1 1) Si for 60 s. A comparison of these two figures clearly indicates that the annealing process resulted in an increase in island

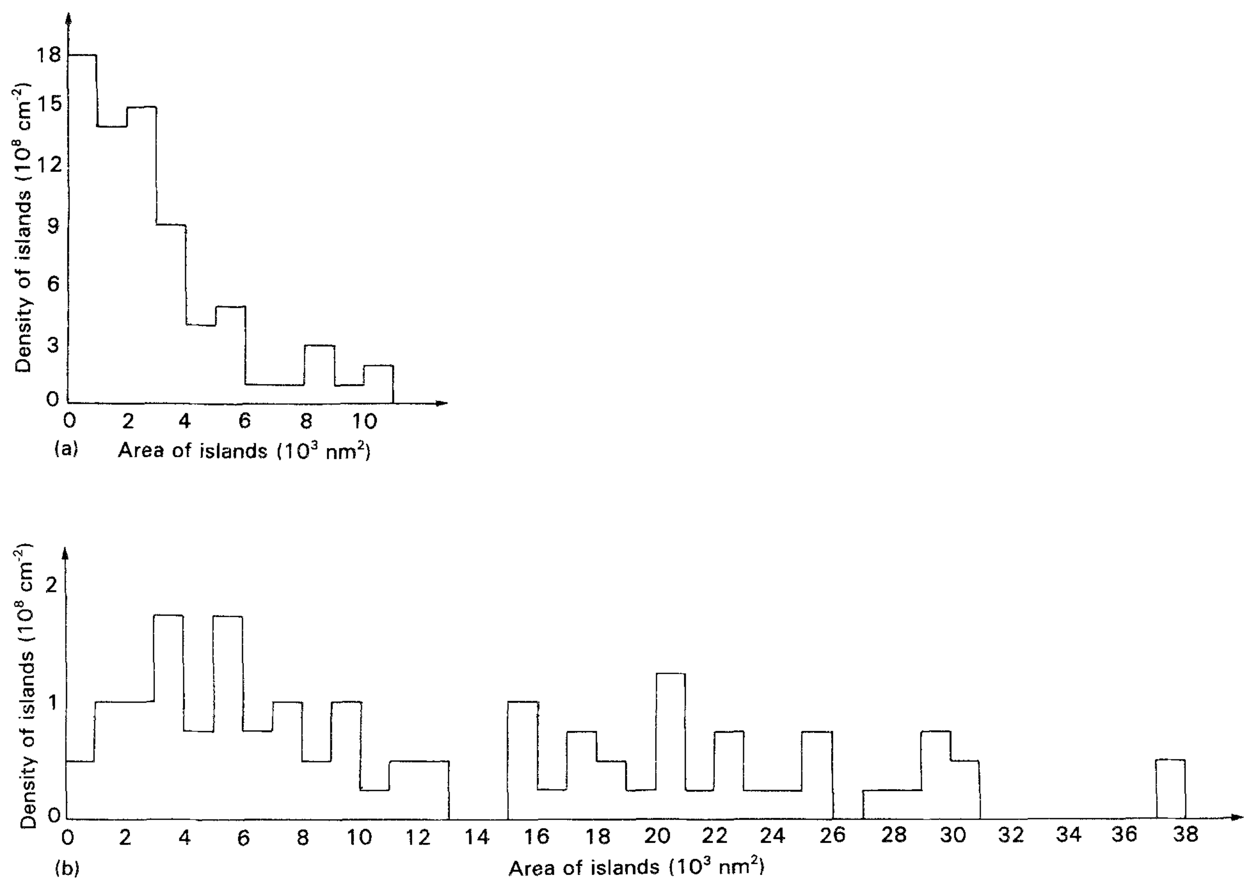
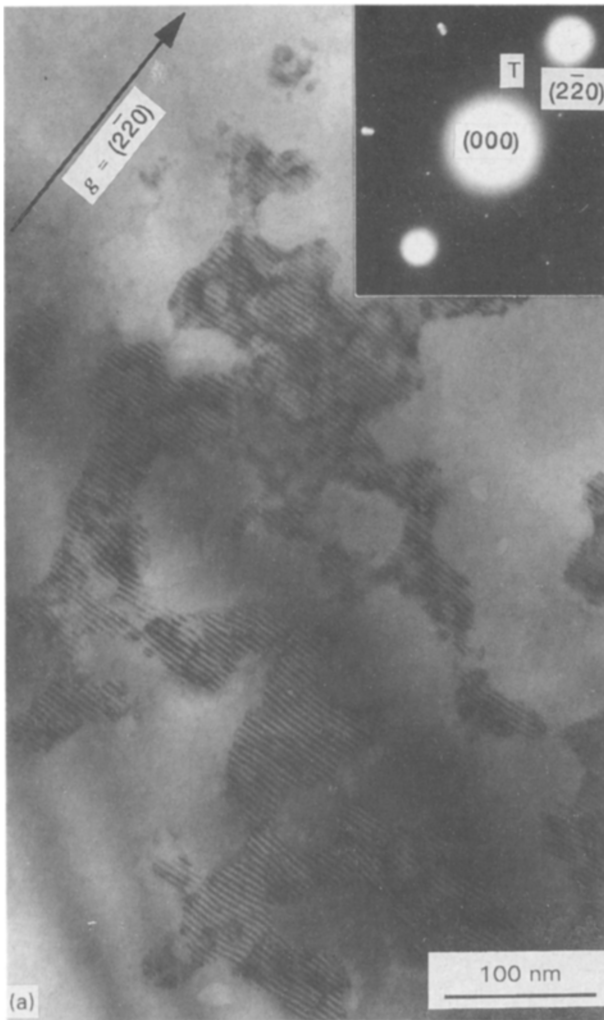


Figure 5 Histograms, showing the (1 1 1) GaAs island size distributions (a) before, and (b) after annealing (720 °C for 10 min) for a growth time of 60 s.



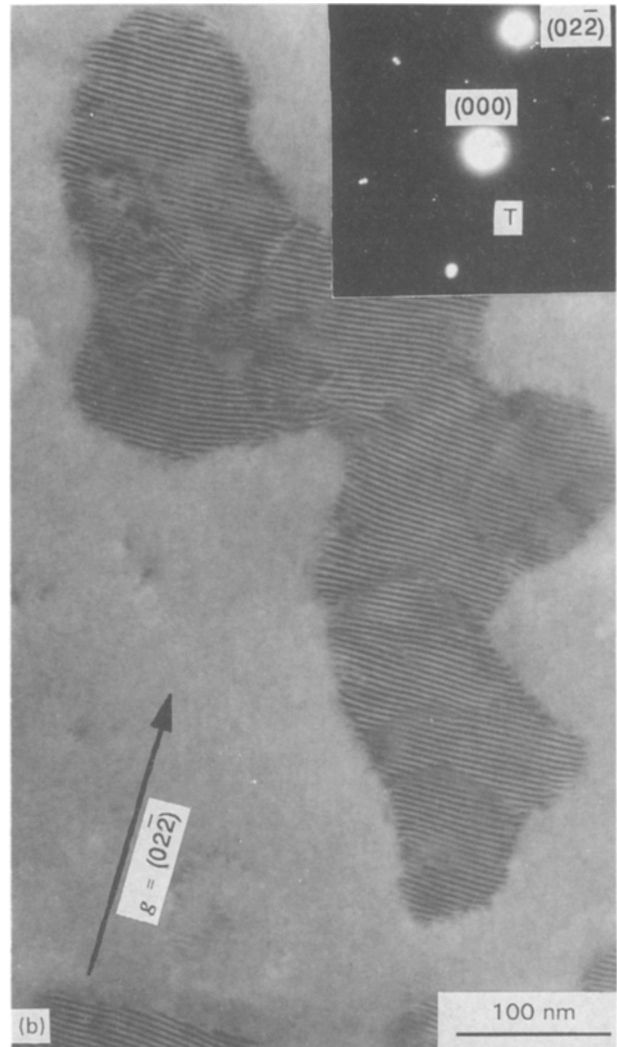
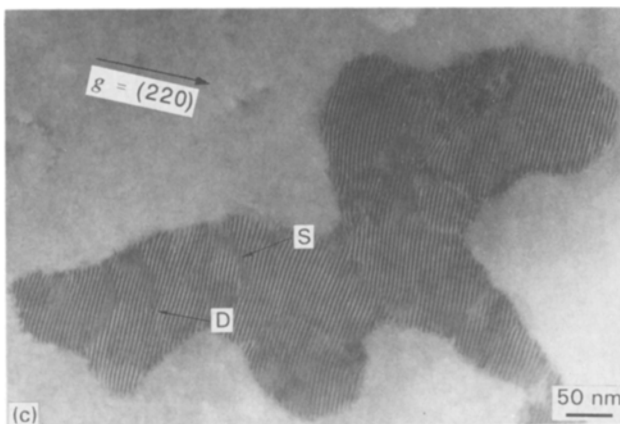


Figure 6 Bright-field planar view TEM images and corresponding SAD patterns of annealed (720 °C for 10 min) MOVPE grown GaAs buffer layers on (1 1 1) Si for growth times of (a) 75, and (b) 90 s. In (c) an enlarged planar view TEM image of an annealed GaAs island, grown for 90 s on Si (1 1 1) at 450 °C, is shown.



size. This is illustrated by the fact that there are fewer islands of sizes $1-3 \times 10^3$ nm^2 after annealing. In addition, the largest as-grown islands measured were in the range 10 000 nm^2 compared to values well over 30 000 nm^2 after annealing.

Fig. 6a shows the annealed (720 °C for 10 min) GaAs buffer layer, which was grown for 75 s. At this stage the GaAs deposit takes on a lacelike appearance with long, narrow channels clearly visible. These narrow channels are created between the islands when they coalesce. Fig. 6b is a planar TEM view of the GaAs buffer layer, grown for 90 s and subsequently annealed at 720 °C for 10 min. The crystallographic profile of this network structure is almost identical to that observed in the annealed layer after 75 s of growth. It is, however, found, as deposition continued from 75–90 s, that the average area of the network structure increased. As already mentioned earlier, moire fringes are ideally suited to allow lattice imperfections to be detected and analysed. In Fig. 6c a planar TEM image of an annealed (720 °C for 10 min) (1 1 1) GaAs island, grown for 90 s at 450 °C, is shown at high magnification. The presence of a threading dislocation (D) and stacking faults (S) are clearly visible in this island. It can be seen from Fig. 6c that a dislocation will appear as an extra "half fringe" on the moiré pattern, as was observed in the present study. In the case of a stacking fault the fringes are mismatched by one-third of a spacing in between the partials. This mismatch represents a stacking fault [15].

Fig. 7a and b shows the as-grown and annealed GaAs buffer layers, respectively, after 120 s of growth. Both these micrographs clearly indicate that continuous GaAs buffer layers are formed after 120 s

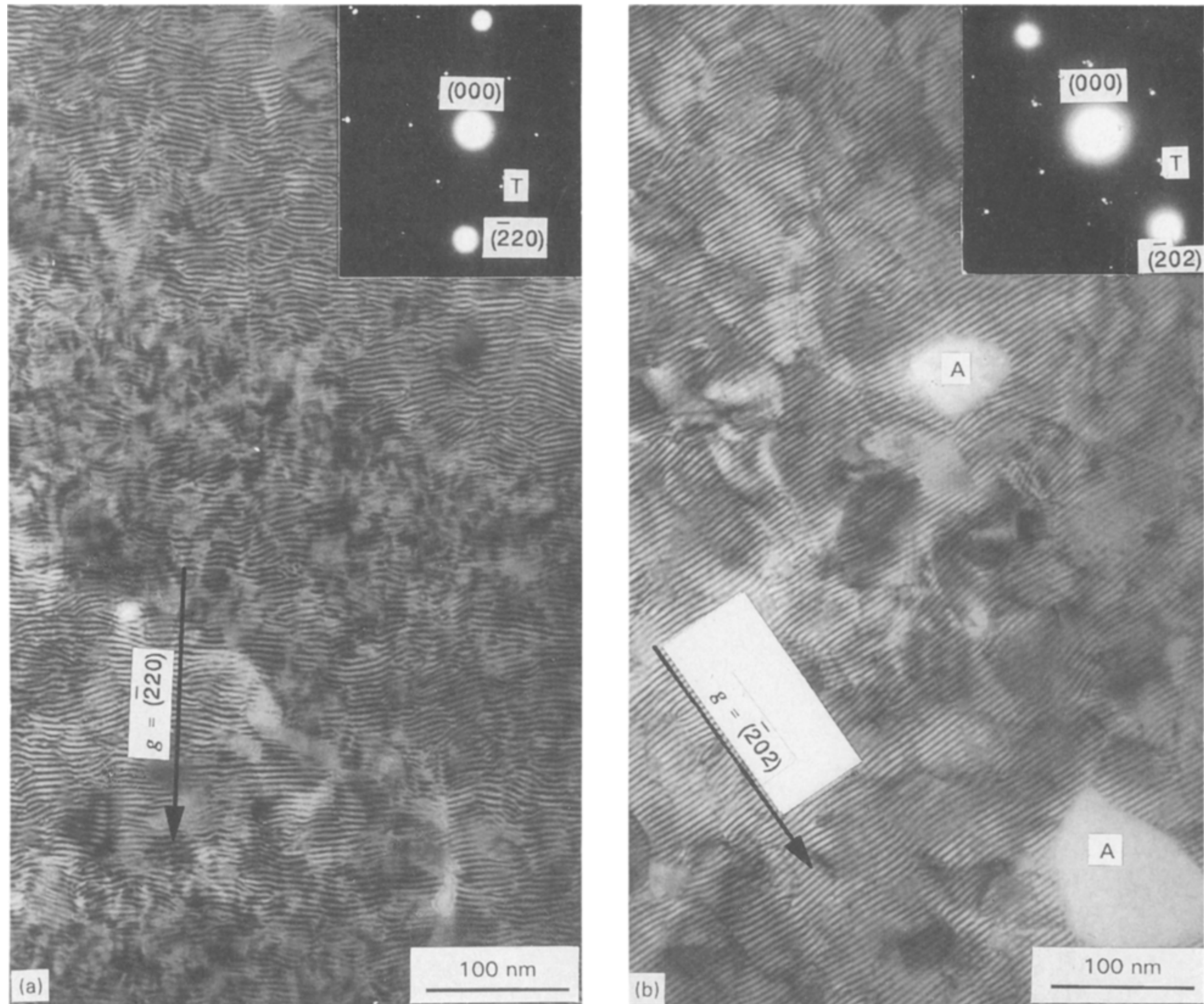


Figure 7 Bright-field planar view TEM micrographs and corresponding SAD patterns of undoped MOVPE (a) as-grown, and (b) annealed GaAs buffer layer on (1 1 1) Si for a growth time of 120 s. The electron beam is close to the ($\bar{1}\,\bar{1}\,\bar{1}$) direction.

of growth. The surfaces of both these layers are almost fully covered with parallel moiré fringes which identifies regions of epitaxially oriented GaAs. Some regions of no moiré fringes contrast are indicated by A in Fig. 7b. The occurrence of these regions can be ascribed to insufficient cleaning of the Si substrate prior to growth [16]. The SAD patterns obtained from the as-grown and annealed GaAs buffer layers, grown for 120 s, are identical [Si and GaAs main diffraction spots and bright (1 1 1) twin reflections]. The high twin spot intensity observed after annealing indicates that thermal annealing at 720 °C for 10 min does not influence the twin structures once a continuous layer has been reached.

4. Conclusion

The study of the initial stages of GaAs growth on Si (1 1 1) indicated that GaAs nucleated as three-dimensional epitaxial islands on the Si substrate. As growth proceeded, these islands expanded until eventually a continuous epitaxial film was formed after 120 s. It was also found that the orientation of the GaAs buffer layers improved during thermal annealing (720 °C for 10 min). This inference was drawn from the fact that the moiré fringes became more regular after annealing. It was also found during this study that thermal annealing changed the structure of the GaAs islands on Si (1 1 1). The annealing process increased the mean size and dispersion of the GaAs islands, while decreasing the number of islands per unit area. TEM studies also indicated that the crystalline quality of the GaAs buffer layers was strongly dependent upon the growth temperature. High temperature (650 °C) grown layers were characterized by the presence of large microtwinned crystallites, yielding rough surface structures. At a low growth temperature (450 °C), however, a high density of small epitaxial islands nucleated on the (1 1 1) Si surface. Selected area diffraction patterns obtained from the GaAs buffer layers showed the presence of extra spots due to secondary twinning on the {1 1 1} planes of GaAs.

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